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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/673,362

09/30/2003

Werner Juengling

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03/23/2005

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP

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EXAMINER

LINDSAY JR, WALTER LEE

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/673,362

Applicant(s)

JUENGLING ET AL.

Examiner

Walter L. Lindsay, Jr.

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 22-30, 33, 70, 71, 74-81, 85, 86 and 92-100 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 70, 71, 74-81, 85, 86 and 92-100 is/are allowed.
- 6) ☒ Claim(s) 22, 23, 25 and 33 is/are rejected.
- 7) ☒ Claim(s) 24 and 26-30 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

This Office Action is in response to an Amendment filed on 1/28/2005.

Currently, claims 22-33, 70-71, 74-81, 84-86 and new claims 92-100. Claims 1-21, 31-32, 34-69, 72-73, 82-83, and 87-91 are canceled.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 22-23 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Son et al. (U.S. 6,383,876 filed 7/27/2000).

Son shows the structure as claimed in Figs. 3a-3j and corresponding text as: a semiconductor substrate (30) (col. 5, lines 57-65); a gate stack (32 and 31) with sidewalls (37) (col. 6, lines 18-22); provided over said substrate, said gate stack comprising: a gate oxide layer (31) provided over said substrate (col. 5, lines 57-65); a polysilicon layer (32) provided over said gate oxide layer (col. 5, lines 57-65); insulating spacers (37) (col. 6, lines 18-22); at least one channel implant region (35) formed underneath said gate stack, wherein said insulating spacers define at least in part the at least one channel implant region (col. 6, line 55- col. 7, line 5); and source and drain regions (38) provided in said substrate on opposite sides of said gate stack (col. 6, lines

Art Unit: 2812

23-33) (claim 22). Son teaches that the insulating spacers are formed on the sidewalls of said gate stack (col. 5, lines 18-22) (claim 23). Son teaches that the at least one channel implant region is defined at least in part by said sidewall spacers and is approximately the same width as said gate stack (col. 6, line 55-col. 7, line 5) (claim 25).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Son et al. (U.S. 6,383,876 filed 7/27/2000) in view of Yu (U.S. Patent No. 6,693,333 filed 5/1/2001).

Son shows the structure substantially as claimed and as described by the preceding paragraphs.

Art Unit: 2812

Son lacks anticipation in not explicitly teaching that: 1) a silicide layer formed over said gate stack, wherein said silicide layer is formed of a material selected from the group consisting of W, WSi_x, WN, Ti, TiN and other combinations thereof (claim 33).

Yu shows a semiconductor-on-insulator circuit with multiple work functions that contains a channel implant. The gate stack (18, 19 and 20) has a silicide layer 26 formed of tungsten silicide formed upon it (col. 5, lines 18-22). The silicide layer 62 is formed above the source/drain regions (23, 25) (col. 6, lines 21-24). The change in work function in helps to allow for adjustments to threshold voltages (col. 3, lines 16-60).

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to modify the structure of Son, by placing silicide on the gate stack and source/drain regions, as taught by Yu, with the motivation that Yu teaches that the changes in the work function in helps to allow for adjustments to threshold voltages.

Allowable Subject Matter

6. Claims 24, 26-30 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 70-71, 74-81, 84-86 and 92-100 are allowed.

8. The following is an examiner's statement of reasons for allowance:

...an insulating layer formed adjacent to said sidewall spacers, said insulating layer and sidewall spacers having etched out upper portions that define an area extending beyond a lateral width of said gate stack, as required by claim 70;

Art Unit: 2812

...second sidewall spacers provided over said conducting layer; and

at least one channel implant region formed underneath said gate stack, which is defined at least in part by said second sidewall spacers, wherein said at least one channel implant region is narrower in width than said gate stack, as required by claim 75;

... an insulating layer formed adjacent to said first sidewall spacers, that define an area extending beyond a lateral width of said gate stack;

a first channel implant region formed underneath said gate stack, which is defined at least in part by said area, as required by claim 80;

...first sidewall spacers provided adjacent to the sidewalls of said gate stack;

a first channel implant region formed underneath said gate stack, which is defined at least in part by said first sidewall spacers;

second sidewall spacers provided over said conducting layer, as required by claim 85; and

...a first set of spacers provided on each side of said gate stack with a second set of spacers provided over said conducting layer; and

a first channel implant region formed underneath said gate stack and in said semiconductor substrate, wherein the first set spacers or second set of spacers define at least in part the width of said channel implant region, as required by claim 92.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

Art Unit: 2812

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

9. Applicant's arguments with respect to claims 22-30, 33 have been considered but are moot in view of the new ground(s) of rejection.

The change in focus from the deposited silicide to the implantation of the channel region, has resulted in the new grounds of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art Unit: 2812

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WLL

March 16, 2005


MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER